





INTERCONNECT STRUCTURE FOR ROOM TEMPERATURE 3D-IC STACKING EMPLOYING BINARY ALLOYING FOR HIGH TEMPERATURE STABILITY

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Outline



- Intro: Current Methods of 3D Assembly
- Proposed Solution: Room Temp Bonding
- Methodology and Characterization
- Evaluation of Experimental Results
- Conclusions and Next Steps



3D Promise / 3D Issues



Promise:

Die #4

H H

HIII

- High speed

Die #5

- Low power

- High density

- Bonding Registration Issues

-Serial Yield Issues

Standard and backside metal layers

Silicon

Device laver

SIP substrate

Circuit board



-Operability/Reliability Issues

Issues:



Assessment of Conventional Reflow and Thermocompression Bonding for 3D-IC

Conventional Reflow and Thermocompression Bonding



Тоо

Red

Much

Here!!

<u>REFLOW</u> (e.g. SnAg/Cu)	THERMOCOMPRESSION (e.g. Cu/Cu)
Fast	Slow
Solder Bridges	Confined, Stable
Low force	High Force
Lateral instability	Laterally Stable
Solder Compliance	Ultra Flatness Required
Unstable during stacking	Thermally Stable
CTE Mismatch	CTE Mismatch
Controlled Atmosphere	Controlled Atmosphere

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Ideal 3D Metallurgy and Bond Process Would Have the Following Characteristics



- High speed bond cycle.
 - Room temperature bond at low force.
 - Air ambient.
- Fine pitch capability (<10µ) without bridging.
- Compliant metallurgy to give flatness margin.
- Unlimited wafer level chip stacking.
 - Mechanical stability during (1+n) bonds.
 - No concerns for oxidation buildup.
- Immune to "next-higher-assembly" reflow.



Proposal: A Novel Metallurgy and Bond Process for <u>Room Temperature</u> 3D Multi-Chip Stacking





- Deoxidized Ag and In bond instantly at RT.
- Compliant Indium allows flatness tolerance.
- Indium has easily controlled squeeze-out.
- Low bonding force: < 0.1 gram per bump at atmospheric ambient.
- Mechanical stability during subsequent bonds.
- InAg alloy anneal is performed at 120-140C (solid state), then stable to >600C.



InAg Binary Bonding-Engineering Details

Detail: Surface Prep

- <u>De-oxidized</u> Indium and Silver will cold-weld instantly at room temp.
- Could wet etch oxide, but thruput is slow and oxide re-grows, making the process time-dependent.
- Atmospheric plasma quickly removes oxide and passivates die for bonding.
- Passivation enables long queue lifetime (hours).





Detail: In-Situ Probing

• Room temp bonding and no confinement enable in-situ probing during bonding.

RT bond, no confinement





Detail: In-Situ Probing

- Room temp bonding and no confinement enable in-situ probing during bonding.
- Operability of each bond can be checked during the stacking operation.

RT bond, no confinement





- Indium and Silver interdiffuse rapidly, even below the melting point of Indium. (~135C)
- Since the bonded connections remain in the solid phase, no compression force is needed during anneal.
 Die flatness/bowing issues are avoided.
- Ideal volume ratio of Ag to In is 2:1 to form Ag₂In with a melting point of ~600C.
- Diffusion kinetics depend on metal purity, time, volume, and temperature.
- Cross-section + EDS provide interdiffusion data.



Experimental

Test Chips







Substrate (<u>Ag bump</u>):

- Silicon substrate.
- 256 Copper daisy chain continuity channels.
- 1280 bumps each.
- Bumps are 4µ dia, 4µ tall
- 10µ centers.
- Copper pillars (plated).
- Nickel barrier (plated).
- Ag cap (plated).





Chip (<u>In bump</u>):

- Silicon chip.
- 256 Copper daisy chain continuity channels.
- 1280 bumps each.
- Bumps are 4µ dia, 4µ tall
- 10 µ centers.
- Copper pillars (plated).
- Nickel barrier (plated).
- In cap (plated).
- No CMP.

Wet Etch Surface Preparation



- Pre-bond wet etch <u>option</u>:
 - Dilute HCL to remove oxidation from Ag and In.
 - Extreme care required to avoid over-etching.
 - Bond parts within 10 minutes to avoid re-oxidation.

Reducing chemistry converts
bump oxide back to native
metal.

- Passivating chemistry ties up metal dangling bonds.
- Process takes less than 1 minute. Atomic passivation inhibits re-oxidation for hours, is bond-able.
- Activates chip surfaces for enhanced underfill wicking.







Room Temperature Bonding

- 27° C substrate and chip.
- Compression bond at <0.1 gram per bump (32Kg total force on 640x512 bumps).
- Maintain 1 μ alignment accuracy thru bonding.
- Confining gas not required.

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• Multiple-chip automatic placement available but not used for these experiments.













- Alloy anneals performed in room air.
- Programmed ramp, temperature, and time.
- **RT-140C** alloy anneal temperature.
- 0-32 Kg compression force applied during anneal.
- 0-30 minutes alloy anneal time.
- Can be performed simultaneously with underfill cure.



Experimental Results

Atmospheric Plasma Cleanup, RT Bond, 200C 10 min Alloy Anneal (no force)



- Strong adhesion of In/Ag as evidenced by tensile rupture.
- Ag2In alloy is <u>ductile</u>, not fragile

 Capable of removing alloyed In/Ag bump from its Ni pad.



Silver-bumped substrate





- No pure Indium remaining.
- Region B is ideal Ag₂In alloy ratio.
- Region C, D & E some Cu, so less Indium available for Ag alloying.
- Cu is probably a remnant of seed layer removal by sputtering. Wet etch next time!
- Nickel barrier (F) shows no diffusion of In, Ag, or Cu.
- Region A is still 96% Ag, indicating a depletion of In for alloying.
- Take-aways:
 - Indium prefers Cu to Ag for alloying.
 - Cu ties up Indium efficiently must eliminate from bonding region.
 - Cu/In intermetallic is reported as fragile – may explain signs of voiding/cracking at original bond interface.





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37.9%

3.3%

65.1%

9.8%

59.0%

7.2%

4.3%

-

0.0%

In

Ni

Cu

32.4%

0.0%

0.0%

100.0%

0.0%

Ni

Cu

-

0.0%

0.0%



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	Α	В	C	D	E	F
Ag	95.7%	67.6%	58.8%	25.1%	33.0%	0.0%
In	4.3%	32.4%	37.9%	65.1%	59.0%	0.0%
Ni	-	-	-	-	-	100.0%
Cu	0.0%	0.0%	3.3%	9.8%	7.2%	0.0%

Makeshift Structure To Avoid Cu Contamination -Replace Ag-Bumped Sub With Ag Planar Coupon





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Ni Barrier

Indium Chip To Silver Coupon; AP Prep RT Bond; Anneal (no force) 30 min/135





InAg alloy separated in bulk



Electrical Continuity Testing

- 256 daisy chain strings per chip.
- 1260 bumps in each string.
- Samples potentially compromised by Cu contamination.

Anneal Temp	Ramp up time	Hold Time	Avg. Ω/bump	Yield to opens	Yield to shorts
135C	20 sec	600 Sec	0.248	98%	98%
190C	60 sec	90 sec	0.108	93%	96%
190C	240 sec	90 sec	0.084	100%	98%



- Increased anneal time/temp appears to improve bump conductance.
- Anneal above Indium melt temp does not seem to affect opens or shorts.
- Limited data suggests capability for low resistance, high yield contact.

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Shear Testing



Anneal Temp	Ramp up time	Hold Time	Shear Strength (Kg)	Shear/ MIL-STD	
135C	20 sec	600 Sec	12.1	242% 🗲	
190C	60 sec	90 sec	8.6	172% 🗲	

- Bonded pairs were shear-tested in accordance with MIL-STD-883 which specifies die shear strength for this size die as 5.0 kg.
- Although shear data is limited, shear strengths on all samples measured did easily exceed the MIL-STD requirement.
- Shear strength is expected to improve when Cu is kept out of bond zone.
- The current data suggest that this bond scheme is capable of robust mechanical performance.

Surface Activation for Capillary Underfill





Die surfaces are not naturally wetting. Contact angle ~50-70

De-oxidizing Atmospheric Plasma also activates die surfaces for enhanced CUF. Contact angle <10



Conclusions



- AgIn system is capable of high speed, low force, room temperature bonding.
- 3DIC stacking at room temperature has significant benefits.
- Metallurgy is capable of MIL-STD mechanical stability following solid-state alloy anneal.
- Copper participates aggressively in Indium metallurgy keep isolated.
- Nickel appears to be a suitable barrier layer to isolate Cu from Ag and In.
- Atmospheric Plasma enables fluxless instant RT bonding of Into-Ag bumps and enhanced wicking of capillary underfills.
- These preliminary results for InAg binary bonding are very encouraging, and warrant further investigation.

Future Plans



- Fabricate new test chips confining the Cu to the interconnect layer.
- Characterize the interdiffusion mechanisms of the Ag/In binary system for small bump volumes.
- Characterize series resistance, shear, and hightemperature stability of the Ag/In binary system.
- Demonstrate multi-chip 3D stacking and subsequent underfill and reflow with the Ag/In binary system.
- Cultivate industrial partnerships to develop and implement this technology.

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